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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,039	12/20/2001	Paul A. Thatcher	10019976-1	2993
7590	01/09/2004		EXAMINER	
HEWLETT-PACKARD COMPANY Intellectual Property Administration P.O. Box 272400 Fort Collins, CO 80527-2400			DESTA, ELIAS	
			ART UNIT	PAPER NUMBER
			2857	

DATE MAILED: 01/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/028,039	THATCHER ET AL.
Examiner	Art Unit	
Elias Desta	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 14 October 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-30 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-30 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) The translation of the foreign language provisional application has been received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). ____ .
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ . 6) Other: ____ .

Response to Applicant's Amendment

Explanation of rejection

Claim rejection – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 8-13, 15-25 and 28-30 are rejected under 35 U.S.C. 102(e) as anticipated by Hamada et al., “A High-Speed Boundary Search SHMOO Plot for ULSI Memories” (IEEE Article, hereafter “Hamada”).

In reference to claims 1 and 21: Hamada teaches a method of testing operational boundaries (see Hamada, Introduction). The method includes:

- Discovering an operational range over a plurality of varying operating parameters for a device by testing points as defined by the plurality of varying operating parameters (see Hamada, Figs 1, 6 and page 5, section 2-1);
- Beginning from known interior operational point [saved pass/fail boundary points in the algorithm of boundary search (fig. 3)] to discover adjacently (pass/fail

points) coupled boundary points that define the operational boundary (see

Hamada, page 5, 1st column, 2nd paragraph); and

- Discovering an operational boundary of the device that includes a plurality of boundary points just outside of the operational range without testing all the plurality of interior operational points (see Hamada, Figs. 9 and 11, page 8, paragraphs 2 and 3).

With regard to claims 2 and 22: as noted above in claims 1 and 21, Hamada further teaches that the method includes an automated search and testing of the operational boundary because Hamada inherently teaches that the algorithm in page 5 is implemented in a computer system to provide a faster search time (see Hamada, page 7, section 3).

With regard to claims 3 and 23: as noted above in claims 1 and 21, Hamada further teaches that varying first and second parameters (see Hamada, Figs. 8 and 9, Shmoo plots have two varying parameters in order to determine a pass or fail point) and hence no other parameter is used in the computation, it is inherent that the remaining parameters are held constant.

With regard to claims 4 and 24: as noted above in claims 1 and 21, Hamada further teaches that the method further includes:

- Beginning from a known interior operational point (see Hamada, Fig. 3, saving pass/fail boundary points information) and testing adjacent points in the first direction until an initial failure point is discovered where the initial failure point is one of the plurality of boundary points (see Hamada, Fig. 9); and

➤ Using the initial failure point, testing for and discovering each of the plurality of boundary points that are adjacently coupled until returning to the initial failure point (see *Hamada*, Fig. 7, the algorithm always has the initial fail point with test value increment).

With regard to claims 5 and 25: as noted above in claims 4 and 24, *Hamada* further teaches that the first direction varies in only one of the plurality of varying parameters in an increasing manner, holding all the remaining parameters constant (see *Hamada*, Table 1, pass/fail test where the second parameter is kept at a value of one or “some constant value “n” for each subsequent boundary condition).

With regard to claims 8 and 28: as noted above in claims 1 and 21, *Hamada* further teaches that the method includes setting an upper and lower limit for each of varying parameters that define operational limits of said operational boundary where points lying outside the operational limits are points of operational failures (see *Hamada*, Fig. 9, “*” represent pass boundary point with upper and lower limit based on the Shmoo grid lines).

With regard to claims 9 and 20: as noted above in claims 1 and 21, *Hamada* further teaches that the method includes setting an upper and lower limit of each of varying parameters that define operational limits as shown in Fig. 9. These limits are set for a memory device, hence it is inherent that the failure points outside the defining operational limits would not be able to boot up and run test applications.

With regard to claims 10 and 30: as noted above in claims 1 and 21, *Hamada* further teaches that the method includes:

- Determining whether the plurality of boundary points is part of an interior fault region with in an operational boundary (see Hamada, Figs. 8 and 9)
- Discovering a second operational boundary of the device that includes a second plurality of boundary points just outside of the operational range of the plurality of boundary points is also part of the interior fault region (see Hamada, Fig. 9, areas in block 1 and 5 of the horizontal plot).

In reference to claim 11: as noted above in claims 3 and 4, Hamada further teaches that the method of testing operational boundaries includes:

- a) Varying a first and second operating parameter in a plurality of operating parameters, where the plurality operating parameters define points in an operating region for a device (see Hamada, Figs. 8 and 9, Shmoo plots have two varying parameters in order to determine a pass or fail point).
- b) Beginning from a known operational point of the device (see Hamada, Fig. 3, saving pass/fail boundary points information), testing adjacently coupled points in a direction until an initial failure point is discovered (see Fig. 9).
- C) Beginning from the initial failure point, testing for and discovering each of a plurality of failure points (see Hamada, Fig. 9) that are adjacently coupled until returning to the initial failure point (since the process is recursive, Fig. 6, test start point selection), the plurality of failure points defining an operational boundary for the device that bounds an operational range including a plurality of interior operational points within the operating region of the device (see Hamada, Fig. 8, Boundary Search Shmoo Plot).

With regard to claim 12: as noted above in claims 2 and 11, Hamada further teaches that the steps (a) through (c) are performed automatically because it is inherent that the algorithm in page 5 of Hamada is implemented in a computer system to provide a faster search time (Hamada, page 7, section 3).

With regard to claim 13: as noted above in claim 11, Hamada further teaches that the direction of the method of testing the operational boundaries of the first variable varies in an increasing manner by holding the remaining parameters constant (see Hamada, Table 1, Boundary Point Data, notice that only "X" value is allowed to vary).

With regard to claims 15 and 16: as noted above in claim 11, Hamada further teaches that the method of testing includes:

d) Discovering if said plurality of failure points bound an interior fault region within the operational range (see Hamada, Fig. 9); further discovering the interior fault region if a last point that has been tested in a set of adjacent points that are examined from the beginning point to an operational limit in the same direction is an operational point (see Hamada, Fig. 7, test start point and Fig. 9 test point).

e) Testing for second plurality of failure points if all of known plurality of interior operational points do not lie with in the plurality of failure points (see Hamada, Figs. 8 and 9); and

With regard to claim 17: as noted above in claim 16, Hamada further teaches that the method includes testing for and discovering each of a second plurality of failure points that are adjacently coupled until returning the last point and the second plurality of failure points defining

a second operational boundary that bounds the operational range within the operating region for the device (see Hamada, Fig. 9, blocks 1 and 5 on the horizontal axis).

With regard to claim 18: as noted above in claim 11, Hamada further teaches that the device described in a memory and a memory is a chip forming an integrated circuit (see Hamada, Abstract).

With regard to claim 19: as noted above in claim 11, Hamada further teaches that the method includes identifying the type of fault at each plurality of failure points (see Hamada, Fig. 9, area where failure test points are attributed).

With regard to claim 20: as noted above in claim 11, Hamada further teaches that the method includes a voltage as an operating parameter (see Hamada, Fig. 12 (d)).

Claim rejection – 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6, 7, 14, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada in view of Huston et al. (U.S. Patent 6,079,038).

In reference to claims 6, 7, 14, 26 and 27: as noted above in claims 4 and 24, Hamada further teaches testing operational boundaries from a known interior operational point (see Hamada, page 6, section 2-3). The method also includes a recursive test start point selection (see

Hamada, Fig. 6). However, Hamada does not teach testing adjacent points in a circular direction starting from known and adjacent interior operational point.

Huston et al. teaches testing adjacent points in a circular direction starting from known and adjacent interior points (see Huston et al., Fig. 17 and column 10, lines 47-52).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the recursive test start selection method as taught by Hamada and incorporate a circular recursive testing method as discussed in Huston et al. in order to provide most definite search method because circular (clockwise or counter-clockwise) recursive method allows the user to explore a three dimensional Shmoo plot with adding too much overhead on the computation time (see Huston et al., column 10, lines 47-65).

Response to Argument

5. In reference to Claims 1 and 21: Unlike Applicants assertion, Hamada et al. teaches a method and apparatus for conducting a boundary search for Shmoo tests on electronic device (ULSI memory devices) (see Hamada et al., Abstract). Hamada et al. further teaches that the test begins from a known interior operational point since the address size in the functional test pattern is established in order to get information about the operating margin (see Hamada et al., page 5, section 2-1). Once this test boundary (pass/fail) is established, the testing of the DUT (device) is conducted from known operating point.

Even though the orientation of the test pattern execution is not mentioned in the claims, Hamada et al. in Fig. 4 b & d describes a diagonal test pattern with an 'x' and 'y' components

that enables the user to implement the Shmoo test in both horizontal and vertical direction (see Hamada et al., page 6, Table 1, boundary point data).

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Desta whose telephone number is (703)-305-3840. The examiner can normally be reached on M-Thu (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)-308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-5841 for regular communications and (703)-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-1782.

Elias Desta
Examiner
Art Unit 2857

-ed

January 7, 2004


MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800